REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

1. Rejection of claims 1-2 as being unpatentable over Okuzono et al. (US 2001/0043178):

Response:

Claim 1:

Claim 1 has been amended to overcome this rejection. Specifically, the limitations "at least two logic circuits have the same function" and "differences among delay time intervals of the timing signals transmitted to different logic circuits **with the same function** less than 1000μs" is added in claim 1. These limitations are fully clearly explicitly, inherently, and implicitly supported in the specification in paragraphs [0018]-[0020] and in Figs. 3-5, and no new matter is introduced. For instance, [0020] describes that the timing control circuit 62 is connected to the first data line driving circuit 56A and the second data lien driving circuit 56B, which are two logic circuits with the same function.

Regarding US 2001/0043178, Okuzono discloses a liquid crystal display. In Okuzono's disclosure, the timing signal VCK is sending to the gate driver 7, and the timing signal SP is sending to the source driver 9, where the gate driver 7 and the source driver 9 are two logic circuits with **different functions** as illustrated in Fig.1. According to claim 1 of the present application, however, the timing signals are sending to logic circuits with **the same function**. Also, the timing delay between different timing signals e.g. between the timing signal VCK and the timing signal SP in Okuzono's teaching is set purposely so as to control operation of an LCD. Specifically, the timing delay between different timing signals in Okuzono's teaching is an ideal value, not an actual value, because Okuzono does not consider the timing delay caused by the relative physical locations between the timing control circuit and other logic circuits receiving the timing signals. In

Okuzono's disclosure, he only teaches sending different timing signals to different circuit circuits with certain intervals. Okuzono does not consider the relative physical locations between the timing control circuit and other logic circuits, and fails to teach or suggest the step of determining the location of the timing control circuit in order to solve the delay time intervals between the timing signals sending from the timing control circuit to different logic circuit with the same function. On the contrary, the method of claim 1 of the present application teaches the limitation "determining a location in the panel for forming the timing control circuit so as to make differences among delay time intervals of the timing signals transmitted to different logic circuits **with the same function** less than 1000μs, and forming the timing control circuit accordingly". Thus, claim 1 is patentably distinct from Okuzono's teaching, and should be allowed reconsideration of claim 1 is politely requested.

Claim 2:

Claim 2 teaches timing signal is transmitted to different logic circuits with the same function by a plurality of transmitting lines, and differences between a product of an equivalent resistance value and an equivalent capacitance value of each transmitting line are less than 1000μs. Since Okuzono only teaches an ideal timing delay between different timing signals sending to different logic circuits with different function, he fails to teach or suggest the physical connection between the timing control circuit and other logic circuits which causes the actual timing delay different from the actual timing delay. Without considering physical connection between timing control circuit and the logic circuits, he fails to teach that the timing signal is transmitted to different logic circuits with the same function by a plurality of transmitting lines, and differences between a product of an **equivalent resistance value** and an **equivalent capacitance value** of **each** transmitting line are less than 1000μs. As a result, claim 2 is patentably distinct from Okuzono's teaching, and should be allowed. Reconsideration of claim 2 is politely requested.

2. Rejection of claims 3-5 as being unpatentable over Okuzono in view of Uehara and in further in view of Kim (US 5,808,596):

Response:

Claim 3:

Claim 3 is dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claim 3 is politely requested.

Claim 4:

Claim 4 teaches the timing signal is respectively transmitted to the first data line driving circuit and to the second data line driving circuit by a first transmitting line and a second transmitting line, differences between a product of an equivalent resistance value and an equivalent capacitance value of the first transmitting line and a product of an equivalent resistance value and an equivalent capacitance value of the second transmitting line being less than 1000μs.

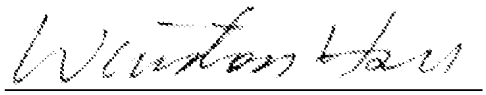
Regarding the cited arts, none of them teaches the limitation "the differences between a product of an equivalent resistance value and an equivalent capacitance value of **the first transmitting line** and a product of an equivalent resistance value and an equivalent capacitance value of **the second transmitting line** being less than 1000μs". Therefore, claim 4 is patentably distinct from the cited arts, and reconsideration of claim 4 is politely requested.

Claim 5:

Claim 5 is dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claim 5 is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



Date: 07/07/2008

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